## 11.1 An 18mW 90 to 770MHz Synthesizer with Agile Auto-Tuning for Digital TV-Tuners

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An 18mW 90 to 770MHz synthesizer is implemented in a low-power mobile receiver for Japanese terrestrial digital broadcasting (ISDB-T for television and ISDB-TSB for radio). The ISDB-TSB bands, 90 to 108MHz (VHFL) and 170 to 222MHz (VHFH), are covered by 3/7MHz steps, and the ISDB-T band, 470 to 770MHz (UHF), by 6MHz steps. We estimate that phase noise less than –80dBc/Hz for offsets below 100kHz with a –20dBc/dec slope over 100kHz is necessary with our RF and IF blocks to meet the specifications for the clock output [1]. We are targeting a 35mW tuner in CMOS, while previous circuits consumed over 150mW [2, 3]. For the synthesizer, we set our target at 20mW. The circuit is fabricated in a 0.11µm CMOS process with a 1.2V power supply.

We focus on simultaneously achieving low power and wide tuning range, and describe the three key blocks, which are shaded in the block diagram shown in Fig. 11.1.1. First, we invented a divide-by-3.5 (DIV/3.5) circuit. Second, we employed two LC-tank VCOs (LC-VCO) that use 7b binary-weighted codes. Finally, we also include an auto-tuning block with an agile tuning method to select the target code of the VCO.

To generate the I/Q phases we use two cascaded divide-by-2 circuits (I/Q-DIV in Fig. 11.1.1). This method is cost effective, as a quadrature-phase LC-VCO for the lower end of the frequency range would require a large on-chip or off-chip inductor. For our pulse-swallow integer-N PLL, we used a 6MHz reference clock to make the PLL bandwidth large enough to suppress the VCO phase noise. Therefore, we need a divide-by-3.5 circuit to achieve both 3/7MHz and 6MHz steps (the following I/Q-DIV block divides by 4). As the power is proportional to the working frequency of the circuit, we invented a new DIV/3.5 circuit that can use the lowest frequency VCO at 2 to 3GHz. If an integer divide-by-7 circuit was used instead of the DIV/3.5, the VCO frequency would have to be 4 to 6GHz. Figure 11.1.2 shows the gate-level schematic and timing diagram of the DIV/3.5. This divider consists of only 4 FFs and 3 NAND gates. We used Yuan and Svensson true single-phase clocked FFs with synchronous set inputs. There are two counters (a top and a bottom) and each of them counts up to seven (the two Q outputs in each counter change in the sequence 10-01-11-00-10-01-00),but they are offset by $^1/_2$ clock cycle since they are driven by complementary clocks . The output is the combination of the two reset pulses, which occur every seventh clock period but are offset, so the net result is a division by 3.5. The duty cycle is corrected to 50% by the next Div/2 of the IQ-DIV block. As all paths are fully symmetric at the transistor level, there is no delay imbalance, which would cause periodic errors in the matching of the quadrature phases. In addition, as this method uses fewer transistors, the delay for the reset that limits the speed is shorter. Power consumption is also small using full inverter logic structures.

As a PLL is sensitive to the noise at the VCO control node, it is good to make the VCO gain as small as possible. Therefore, we adopted multiple-step VCO structures [3]. As shown in Fig. 11.1.3, we used 6b binary-weighted MIM capacitors with transistor switches for coarse-tuning, and varactors for fine-tuning. By using varactors, the PLL can precisely lock to a target frequency without using complex digital blocks [4]. We also separated the VCO into two VCOs, a high- and a low-frequency VCO (VCOH, VCOL), which have different inductors. If we used one inductor to cover the wide frequency range, we would have to use a larger variable capacitor and would need more current to sustain a large oscillation amplitude. By using two appropriate inductors we reduced power consumption. By coarse-tuning switches (codes) provide 128 discrete steps. The measured results for both VCOs are also shown in Fig. 11.1.3. VCOL oscillates from 1.50 to 2.48GHz and VCOH oscillates from 2.20 to 3.78GHz. Overlap between the steps and each VCO guarantees continuous frequency coverage, even with process, voltage, and temperature variations. The phase noises at 100kHz offset are –91 and –90 dBc/Hz for VCOL and VCOH respectively.

To use multiple-step VCOs in a synthesizer, the coarse-tuning codes must be automatically selected to yield the closest discrete frequency. The codes are selected by the auto-tuning block, which is designed using a new dynamic binary-branch method. Figure 11.1.4 shows a simplified block diagram and flowchart for the auto-tuning circuit. The important parts are the COMP and CNTRL blocks. In order to handle asynchronous count errors between the two counters, the timing of each gating trigger (when the COMP checks the difference between the two inputs) uses unequal intervals to avoid mistakes when judging closeness to the target frequency. During the test of each code, the judging of the high or low is repeated while the difference is kept less than 2 by considering the asynchronous counting. The more each clock frequency is separated, the earlier they shift to the next test, and if the counters arrive at the last judgment point and get a difference less than 2, this terminates the rest of the auto-tuning process. In the conventional method, we judge only at a single constant timing (this timing is close to our last gating trigger timing) for each test. The period used in the conventional method is inversely proportional to the minimum frequency difference between each step, therefore the tuning time increases when more steps are used and they become smaller. This dynamic method roughly improves the speed by the factor of 'total bits –2', as only the last one or two tests select the code that is close to the target and need a longer period to finish judging. Figure 11.1.5 shows the measurement results for the auto-tuning process. After selecting the target codes by the six tests of different periods, the CNTRL closes the PLL loop. This auto-tuning block uses about 1500 gates and takes only 0.03mm$^2$.

Figure 11.1.6 shows the phase noise of the quadrature output. Three pairs of curves are shown, one pair for each band; VHFL, VHFH and UHF. Each pair of curves represent the measured phase noise at the lowest and highest frequency settings for each band. Phase noise is lower than –100dBc/Hz at 100kHz offset. Die micrographs are shown in Fig. 11.1.7. The synthesizer is 1.9mm$^2$, including the LPF for the PLL. The main features of the synthesizer are also summarized in Fig. 11.1.7. The synthesizer achieves the wide target tuning range and the desired phase noise with a total power consumption of 18 to 20mW.

*Acknowledgments:*
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*References:*
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[2] D. Saias et al., "A 0.12µm DVB-T Tuner," *ISSCC Dig. Tech. Papers*, pp.430-431, Feb. 2005
[3] H. van Rumpt et al., "UMTV: a Single Chip TV Receiver for PDAs, PCs, and Cell Phones," *ISSCC Dig. Tech. Papers*, pp.428-429, Feb., 2005
[4] R. B. Staszewski et al., "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol 39, no 12, pp.2278-2291, Dec., 2004.

 

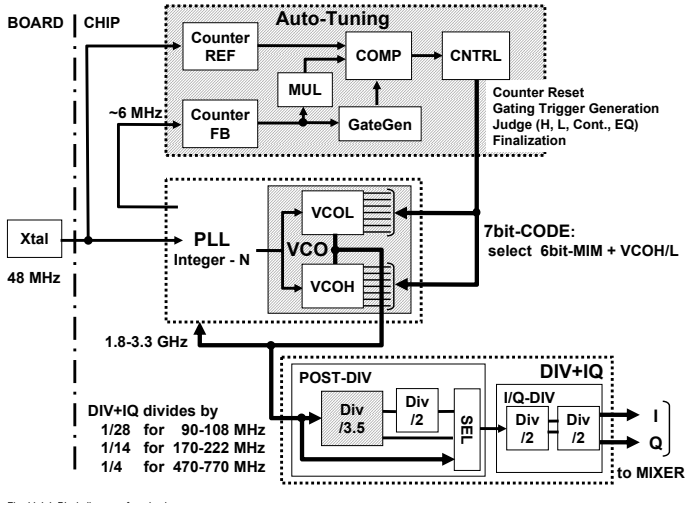


Figure 11.1.1: Block diagram of synthesizer.

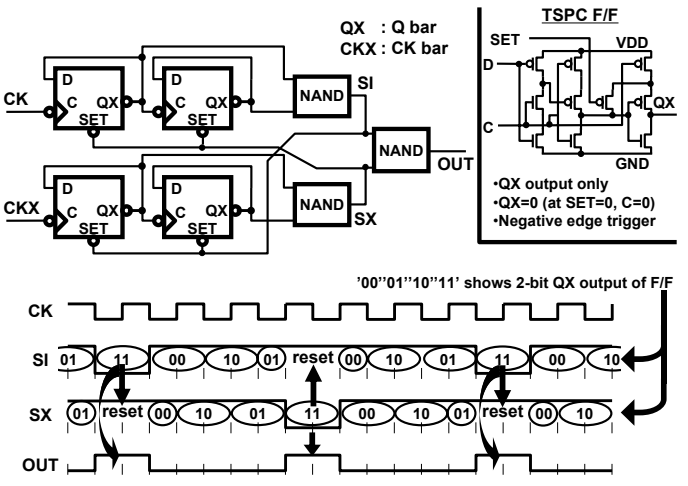


Figure 11.1.2: Simplified block and timing diagrams of DIV/3.5.



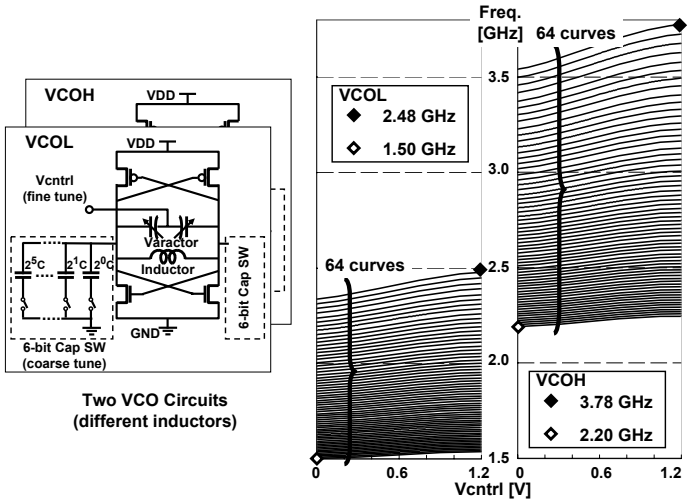


Figure 11.1.3: VCO circuit and measured frequency curves.

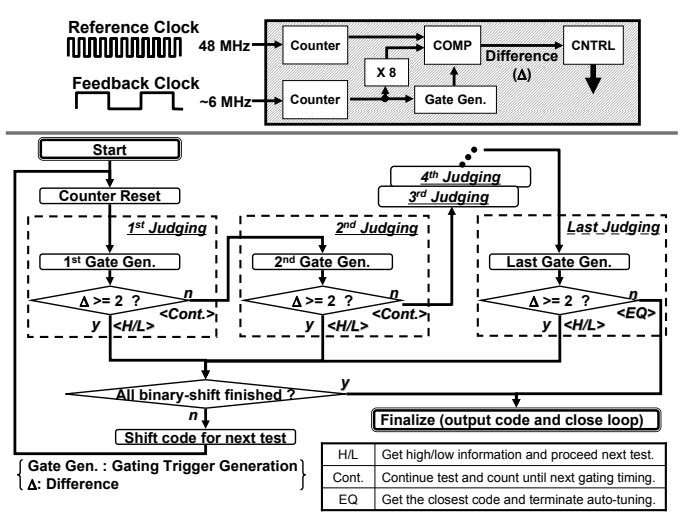


Figure 11.1.4: Auto-Tuning flow chart.

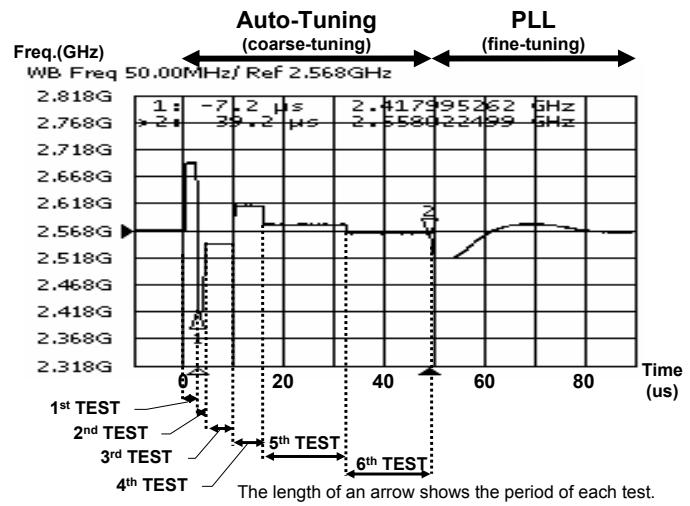


Figure 11.1.5: Measured Auto-Tuning process.

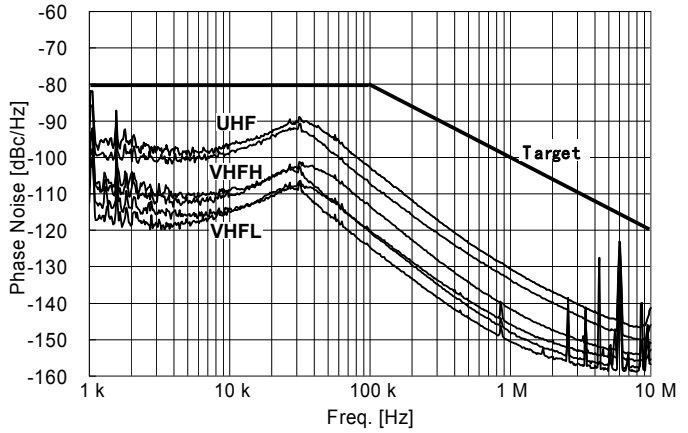


Figure 11.1.6: Measured phase noise of quadrature output.

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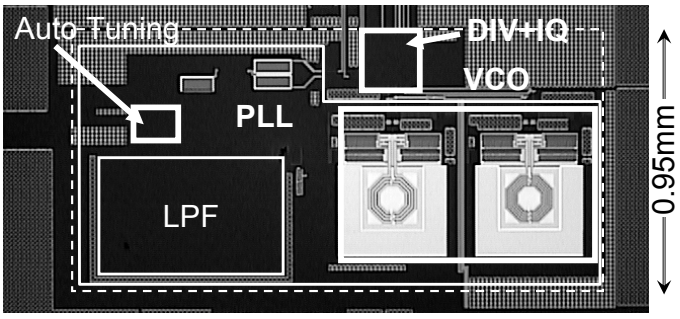


| Technology | 0.11 μm CMOS | Range | 90-770 MHz |
|---|---|---|---|
| Supply voltage | 1.2 V | Resolution | |
| Current | 15.3-16.9 mA | 90-220 MHz | 428 kHz |
| Chip area | 1.9 mm² | 470-770 MHz | 1.5 MHz |
| Reference freq. | 6 MHz | Phase noise | <-100 dBc/Hz at 100 kHz |

**Figure 11.1.7: Chip micrograph.**

 